

# 1.5V Drive Pch MOSFET

## QS8J2

### ● Structure

Silicon P-channel MOSFET

### ● Features

- 1) Low On-resistance.
- 2) High power package.
- 3) 1.5V drive.

### ● Application

Switching

### ● Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS8J2		○

### ● Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit	
Drain-source voltage	$V_{DSS}$	-12	V	
Gate-source voltage	$V_{GSS}$	±10	V	
Drain current	Continuous	$I_D$	±4	A
	Pulsed	$I_{DP}$ *1	±12	A
Source current (Body Diode)	Continuous	$I_s$	-1	A
	Pulsed	$I_{sp}$ *1	-12	A
Power dissipation	$P_D$ *2	1.5	W / TOTAL	
		1.25	W / ELEMENT	
Channel temperature	Tch	150	°C	
Range of storage temperature	Tstg	-55 to +150	°C	

\*1  $P_w \leq 10\mu s$ , Duty cycle  $\leq 1\%$

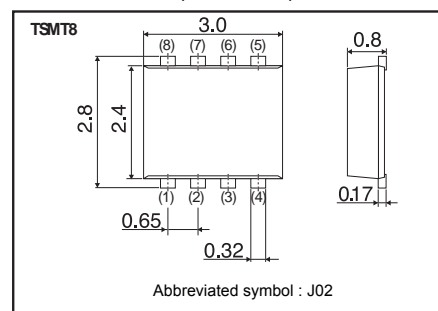
\*2 Mounted on a ceramic board.

### ● Thermal resistance

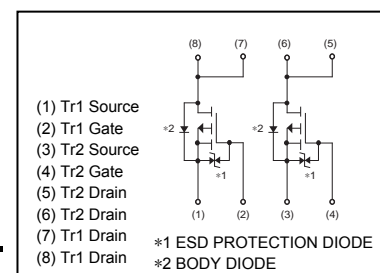
Parameter	Symbol	Limits	Unit
Channel to Ambient	$R_{th}(ch-a)$ *	83.3	°C/W / TOTAL
		100	°C/W / ELEMENT

\* Mounted on a ceramic board.

### ● Dimensions (Unit : mm)



### ● Inner circuit



● **Electrical characteristics** (Ta = 25°C)

<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	$I_{GSS}$	-	-	±10	μA	$V_{GS}=\pm 10V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	-12	-	-	V	$I_D=-1mA, V_{GS}=0V$
Zero gate voltage drain current	$I_{DSS}$	-	-	-1	μA	$V_{DS}=-12V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	-0.3	-	-1.0	V	$V_{DS}=-6V, I_D=-1mA$
Static drain-source on-state resistance	$R_{DS(on)}$	-	26	36	mΩ	$I_D=-4A, V_{GS}=-4.5V$
		-	36	50		$I_D=-2A, V_{GS}=-2.5V$
		-	46	69		$I_D=-2A, V_{GS}=-1.8V$
		-	66	132		$I_D=-0.8A, V_{GS}=-1.5V$
Forward transfer admittance	$ Y_{fs} ^*$	5.5	-	-	S	$I_D=-4A, V_{DS}=-6V$
Input capacitance	$C_{iss}$	-	1940	-	pF	$V_{DS}=-6V$
Output capacitance	$C_{oss}$	-	260	-	pF	$V_{GS}=0V$
Reverse transfer capacitance	$C_{rss}$	-	240	-	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}^*$	-	10	-	ns	$I_D=-2A, V_{DD}=-6V$
Rise time	$t_r^*$	-	60	-	ns	$V_{GS}=-4.5V$
Turn-off delay time	$t_{d(off)}^*$	-	300	-	ns	$R_L=3\Omega$
Fall time	$t_f^*$	-	180	-	ns	$R_G=10\Omega$
Total gate charge	$Q_g^*$	-	20	-	nC	$I_D=-4A, V_{DD}=-6V$
Gate-source charge	$Q_{gs}^*$	-	3.5	-	nC	$V_{GS}=-4.5V, R_L=1.5\Omega$
Gate-drain charge	$Q_{gd}^*$	-	3.0	-	nC	$R_G=10\Omega$

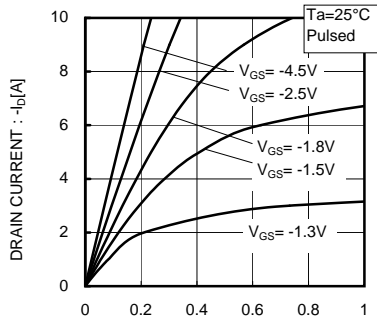
\*Pulsed

● **Body diode characteristics** (Source-Drain) (Ta = 25°C)

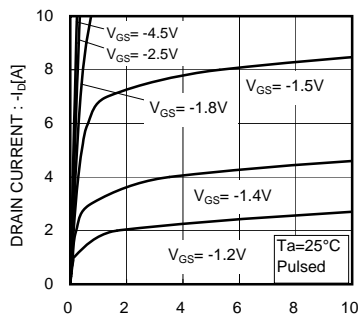
<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	$V_{SD}^*$	-	-	-1.2	V	$I_S=-4A, V_{GS}=0V$

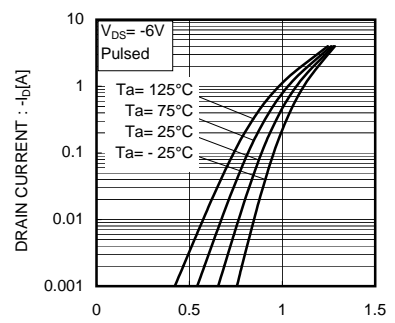
\*Pulsed



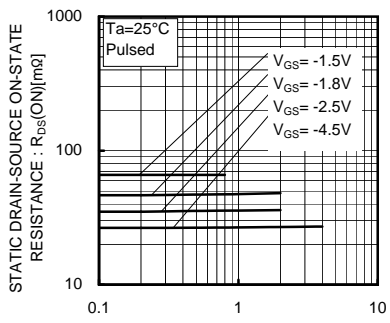
DRAIN-SOURCE VOLTAGE : -V<sub>DS</sub>[V]  
Fig.1 Typical output characteristics ( I )



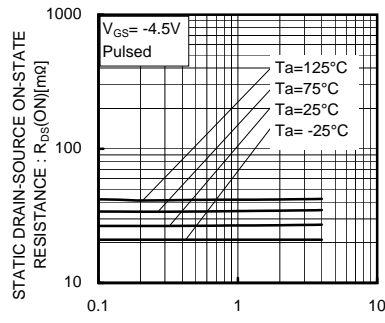
DRAIN-SOURCE VOLTAGE : -V<sub>DS</sub>[V]  
Fig.2 Typical output characteristics( II )



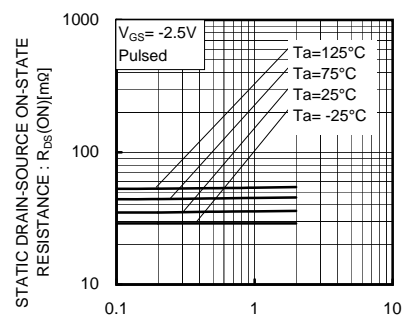
GATE-SOURCE VOLTAGE : -V<sub>GS</sub>[V]  
Fig.3 Typical Transfer Characteristics



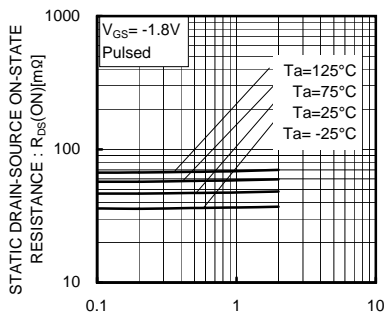
DRAIN-CURRENT : -I<sub>b</sub>[A]  
Fig.4 Static Drain-Source On-State Resistance vs. Drain Current ( I )



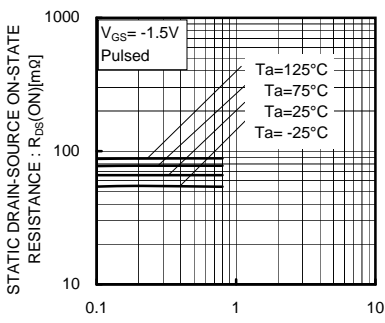
DRAIN-CURRENT : -I<sub>b</sub>[A]  
Fig.5 Static Drain-Source On-State Resistance vs. Drain Current( II )



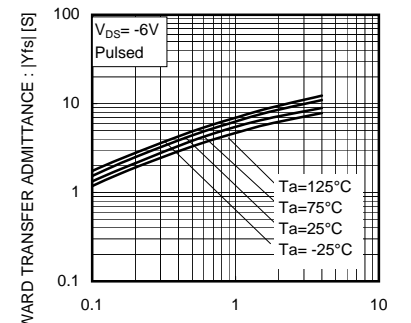
DRAIN-CURRENT : -I<sub>b</sub>[A]  
Fig.6 Static Drain-Source On-State Resistance vs. Drain Current( III )



DRAIN-CURRENT : -I<sub>b</sub>[A]  
Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)



DRAIN-CURRENT : -I<sub>b</sub>[A]  
Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(V)



DRAIN-CURRENT : -I<sub>b</sub>[A]  
Fig.9 Forward Transfer Admittance vs. Drain Current

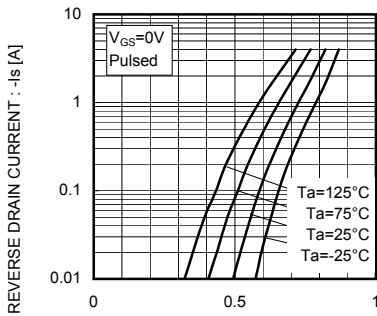


Fig.10 Reverse Drain Current vs. Source-Drain Voltage

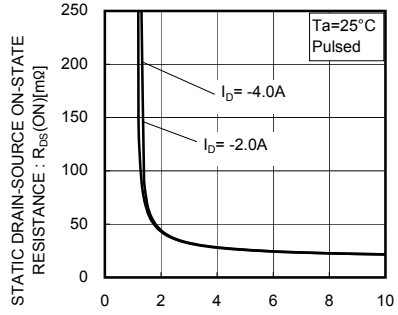


Fig.11 Static Drain-Source On-State Resistance vs. Gate Source Voltage

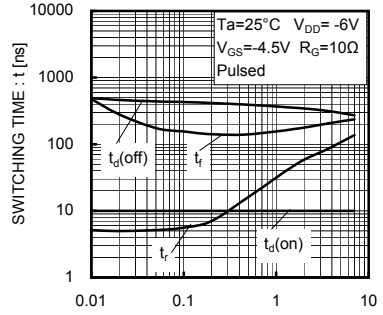


Fig.12 Switching Characteristics

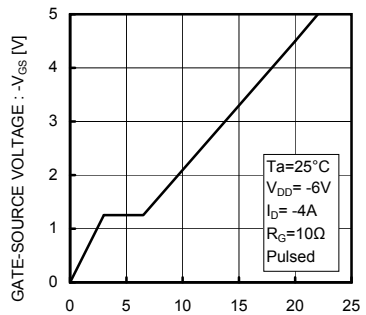


Fig.13 Dynamic Input Characteristics

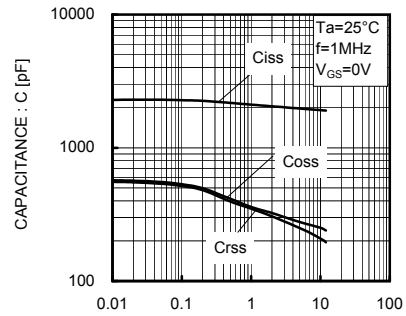


Fig.14 Typical Capacitance vs. Drain-Source Voltage

● Measurement circuits

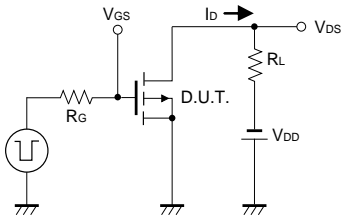


Fig.1-1 Switching Time Measurement Circuit

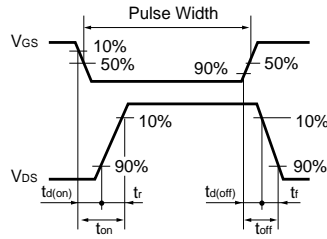


Fig.1-2 Switching Waveforms

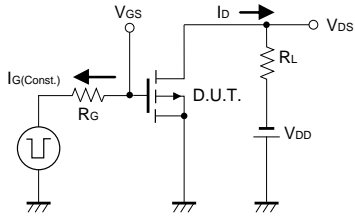


Fig.2-1 Gate Charge Measurement Circuit

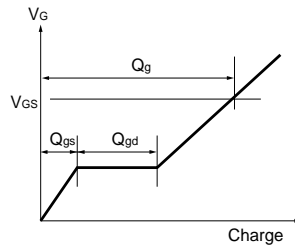


Fig.2-2 Gate Charge Waveform

● Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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